REMARKS

A. GENERALLY

Claims 1-14 remain in the Application. Claims 1, 8 and 11-13 have been amended. No new matter has been added.

B. CLAIMS REJECTIONS

1. Claim Rejections Pursuant to 35 U.S.C. § 102

Claims 1-14 have been rejected under 35 U.S.C. 102(a) as being anticipated by European Patent Application EP0690370 filed by Cohen (hereinafter, "Cohen").

Claim 1 (as amended) recites the following limitations:

1. (Currently Amended) A microcontroller the programming of which is carried out in at least one machine-dependent assembler language in which the assembler commands, with the exception of conditional program jumps or program branches, respectively, are executed independently of data, comprising at least one random number generator assigned to the microcontroller, by means of which the program jumps and program branches are executed in dependence on the state of the random number generator and independently of the internal state of the programming of the microcontroller.

The Office Action asserts that the disclosures at page 9, lines 10-25 and claims 9 and 10 teach these limitations. Applicant respectfully disagrees.

Cohen generally describes a processor that is capable of mimicking an existing processor. Various solutions to adjusting timing differences between the processor and the mimicked processor are described.

Cohen also describes a method for performing a "robust" conditional jump. The contents and the integrity of a condition are determined. If the condition signal indicates that the integrity of the condition is not maintained, a jump to a first location is executed. If the condition signal indicates that the integrity of the condition is maintained and the condition is fulfilled, a jump to a second location is executed. If the condition signal indicates that the integrity of the condition is maintained and the condition is not fulfilled, a jump to a third location is executed. (See, Cohen, p. 3, lines 39-44.) The process is further described at page 9, lines 10-25 and claim 9 of Cohen as cited by the examiner in rejecting claim 1 (as amended) hereof.

Cohen also describes a memory access apparatus including a pseudo-random access delay signal generator generating an access delay signal which is at least pseudo-random and

which determines the number of clock cycles to elapse from a memory access instruction clock cycle to actual memory access, and a memory access unit receiving the access delay signal and operative to access the memory after the number of clock cycles has elapsed. (See, Cohen, p. 3, lines 45-51.) The access apparatus is further described in claim 10 of Cohen as cited by the examiner in rejecting claim 1 (as amended) hereof.

Applicant respectfully submits that the cited disclosures of Cohen do not teach the execution of program jumps in dependence on the state of the random number generator. The jumps disclosed by Cohen at page 9, lines 10-25, and claim 9 are dependent on the integrity and fulfillment of a condition as determined by a condition signal. The jump is not disclosed as being determined in dependence on the state of a random number generator.

> The apparatus of Fig. 7 includes a conditional jump unit 450 which is operative in response to an actuating "perform robust conditional jump" signal received from an instruction decoder 460.
>
> A composite condition signal is received from a suitable source (not shown), either internal or external. The composite condition signal includes a condition component which determines the jump and an integrity component which allows the integrity of the composite condition signal to be verified. For example, the integrity component may include a copy of the condition component and/or may include the l's complement of the condition component and/or may include humming error detection code or any other suitable error detection code. The complexity of the integrity component depends on the required degree of confidence in the integrity of the composite condition signal.
>
> The jump unit 450 is operative to perform the following operations:
>
> a. testing the contents and the integrity of the composite condition signal within a single machine cycle;
>
> b. jumping to a first location (go_error) if the condition signal indicates that the integrity of the condition is not maintained;
>
> c. jumping to a second location (do_jump) if the condition signal indicates that the integrity of the condition is maintained and the condition is fulfilled; and
>
> d. jumping to a third location, such as, for example, the immediately following location instruction (do_not_jump) if the condition signal indicates that the integrity of the condition is maintained and the condition is not fulfilled. (Cohen, p. 7, line 41 through p. 8, line 4.)

The Office Action asserts that this limitation is met by the disclosure of Cohen of a memory access apparatus including a pseudo-random access delay signal generator generating an access delay signal.

> Cohen describes the access apparatus as follows:
>
> The timing diagram of Fig. 8B illustrates a delay between the memory request to the memory access whose duration, "delay time", is preferably pseudo-random or even random. Preferably, the range of the pseudo-random or random delay duration is programmable. Preferably, the duration of the memory access signal, "access time" is also programmable.
>
> The memory cycle time is measured from the initiation of the memory request signal to the termination of the memory cycle completion signal supplied to the execution unit 470 by the memory controller 480 (as demonstrated by the prior art embodiment of Fig. 9). Preferably, the memory cycle time is programmable. In this case, there is typically a second delay period extending from termination of the memory access signal to the beginning of the memory cycle completion signal. The length of the second delay period is the user-selected duration of the memory cycle, minus the sum of the duration of the memory request signal, the pseudo-random/random delay time, the access time, and the duration of the memory cycle completed signal. (Cohen, p. 9, lines 39-48.)

Cohen teaches establishing an access delay signal which is at least pseudo-random and which determines the number of clock cycles to elapse from a memory access instruction clock cycle to actual memory access. Cohen does not suggest that the output of the random number generator may be used to control a jump command.

The Office Action asserts that the robust jump program listing disclosed by Cohen at p. 9 teaches that the conditionbit and RequestJump parameter are driven by a pseudo random generator signal. Applicant respectfully submits that the listing does not support this conclusion. Rather, Cohen states that:

> A particular feature of the apparatus of Fig. 7 is that the jump location is determined within the same cycle as the integrity check such that it is impossible for the composite condition component signal to lose its integrity after the integrity check and before the jump location is determined. (Cohen, p. 9, lines 6-8.)

Based on the foregoing, claim 1 (as amended) recites limitations that are not taught by Cohen. Claim 1 (as amended) is not, therefore, anticipated by Cohen.

Claims 2-4 and claim 10 (as amended) depend from claim 1 (as amended) and recite all of the limitations of that base claim. Based on the foregoing, claims 2-4 and 10 recite limitations not taught or reasonably suggested by Cohen and are not anticipated by that reference.

Claim 5 has been rejected on the same grounds as claim 1 (as amended). For the reasons set forth in the discussion of claim 1 (as amended), claim 5 recites limitations not taught or reasonably suggested by Kocher and is not anticipated by that reference.

Claims 6-9 depend directly or indirectly from claim 5 and recite all of the limitations of that base claim. Based on the foregoing, claims 6-9 recite limitations not taught or reasonably suggested by Kocher and are not anticipated by that reference.

Claim 11 (as amended) recites the following limitations:

11. (Currently Amended) A microcontroller comprising:

a central processing unit;

a memory accessible to the central processing unit, wherein the memory comprises instructions and wherein the central processing unit is configured for:

accessing the instructions, wherein the instructions comprise different instruction sequences for accomplishing a same desired action and where each different instruction sequence produces a same result value for a same input value;

receiving a random number associated with one of the different instruction sequences;

receiving the same input value; and

executing the one of the different instruction sequences associated with the random number using the same input value to produce the same result.

Claim 11 has been rejected as being anticipated by Cohen. Claim 11 (as amended) recites the limitations, "accessing the instructions, wherein the instructions comprise different instruction sequences for accomplishing a same desired action and where each different instruction sequence produces a same result value for a same input value," and "receiving a random number associated with one of the different instruction sequences."

Applicant submits that Cohen does not teach associating instruction sequences that produce a same result with a random number as recited in claim 11 (as amended). Rather, as discussed with respect to claim 1 (as amended), Cohen describes using a random number generator to establish the number of clock cycles to elapse from a memory access instruction clock cycle to actual memory access.

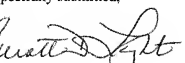
Based on the foregoing, claim 11 (as amended) recites limitations that are not taught by Cohen. Claim 11 (as amended) is not, therefore, anticipated by Cohen.

Claims 12-14 as currently listed depend from claim 11 (as amended) and recite all of the limitations of that base claim. Based on the foregoing, claims 12-14 recite limitations not taught or reasonably suggested by Cohen and are not anticipated by that reference.

E. CONCLUSION

Applicant respectfully submits that the claims as currently listed are in condition for allowance. Applicant requests that this response be entered and that the current rejections of the claims now pending in this application be withdrawn in view of the above amendments, remarks and arguments.

Respectfully submitted,



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